Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OFFSET NULL**
2. **INPUT –**
3. **INPUT +**
4. **V –**
5. **OFFSET NULL**
6. **OUTPUT**
7. **V +**
8. **STROBE**

**.066”**

**3 4 5 6**

**1 8 7**

**2**

**MASK**

**REF**

**.063”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” min**

**Backside Potential: V-**

**Mask Ref: 13857**

**APPROVED BY: DK DIE SIZE .063” X .066” DATE: 8/30/21**

**MFG: INTERSIL / HARRIS THICKNESS .021” P/N: CA3140**

**DG 10.1.2**

#### Rev B, 7/19/02